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Integration of Silicon with Passive Devices Yields Advantages in Wireless Design

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This article describes a new design tool for integrating RF passive component design at the chip and package level, reducing overall size, minimizing external components and improving performance

The wireless market presents conflicting demands to the RF system developer. Multi-band and multi-mode operation must be provided with improved RF performance, using less power, in a highly integrated form factor and, of course, at a lower system cost. These conflicting demands may be realized through the fusion of high quality, high tolerance RF passive components configured from package interconnects as well as metalization layers in advanced silicon processes such as RF CMOS and SiGe BiCMOS. This paper presents a brief overview of a unique approach to complex RF designs, employing a passives-based design methodology aided by specialized EDA tools.

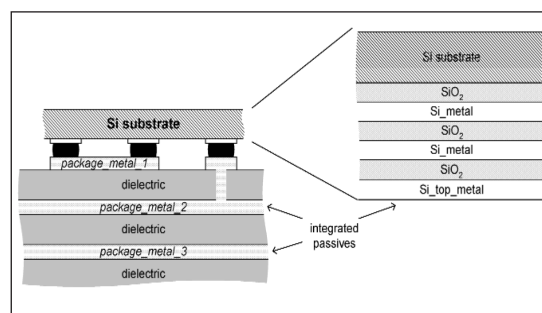

Figure 1 · Silicon and in-package passives.

Integrated RF System Design

To RF system and silicon designers, the semiconductor package has been considered a "necessary evil" due to resistive and reactive losses. The outstanding performance of SiGe and other high-speed processes is often seriously degraded by the parasitic impedances of the package. Although a silicon chip may show excellent performance at a probe station, once placed in its housing (the package) the performance is often seriously compromised. Furthermore, the on-chip interconnects that interface the RF circuit with the package often worsen its performance in ways that conventional circuit simulators cannot easily predict.

It is now possible to actually use the on-chip and package interconnects as part of the overall system-level circuit (Figure 1), thus realizing a two-step improvement—accurately quantifying the parasitic responses of on-chip and in-package wiring, and actually using the metal layers in the package and on the silicon die as part of the circuit design. This new approach has several key advantages:

- The passive devices can be optimized for a given silicon design
- Reduced power consumption by reducing package parasitic reactance losses
- Lower susceptibility to interference and spurious radiation with filters and resonators much closer to the active silicon chip
- Multi-band and multi-mode systems can be more easily realized by switched passive filters and resonators
- Frequency-determining passive components (package option) allow a single silicon chip to operate over an extended range of frequencies, allowing a complex system design to be changed to a different operating frequency quickly
- Smaller overall form factors (fewer external components)
- Lower overall system cost

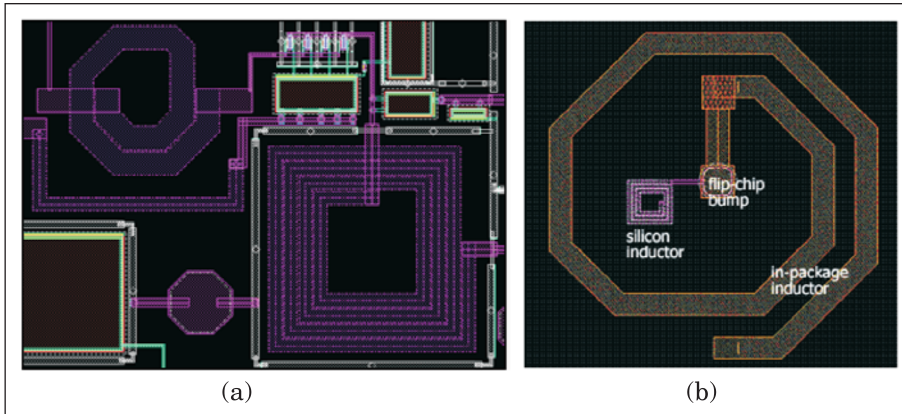

Figure 2 · Passives modeling environment: (a) on-chip, (b) silicon-in-package.

HELMET: A Passive Component Modeling Platform

To enable this new design approach, Helic, in collaboration with Atmel, has developed HELMET, a custom design platform which transcends, yet complements existing design software tools such as Agilent's Momentum™ and Ansoft's HFSS™. While these tools provide accurate passive models based on variations of the MoM (Method of Moments or Finite Element techniques), the computation times required for simulating complete multi-layered circuits may be several hours or days, depending on the system under test. Such long simulation times can render these tools impractical for many design schedules.

In contrast, HELMET permits accurate full model extraction of the silicon working with on-chip and in-package passives in just a few seconds. Subsequently, the generated model netlist can be simulated with any SPICE-type circuit simulator. This dramatically reduces the design time and number of silicon and package test runs required to optimize a system.

The tool accurately models the coupling effects among all metal elements on the die and in the package. Thus, cross-coupling effects are accurately modeled and the results are calculated in seconds, even with numerous passive elements and complex metal interconnects. In effect, the tool "doesn't care" if the metal elements are "intentional" or "parasitic," lumped or distributed. Element values and all cross-coupling effects are simulated simultaneously with the active part of the circuit. Consequently, the semiconductor design/simulation platform becomes a tool for the entire system: from antenna input to base-band output.

Helic's core inductor modeling engine has been validated across several silicon and non-silicon processes. Its unique features include:

- Scalable, frequency-dependent models for spirals
- Modeling of magnetic coupling (mutual inductance) among multiple inductors
- Applicable to silicon and compound MMIC, ceramic and organic laminate processes
- Unified interface for chip-package co-design
- SPICE-compatible RLCK netlist models for rapid extraction and simulation
- Rapid simulation times, compared to EM tools

HELMET Design Environment

HELMET is a custom-made EDA tool developed by Helic for Atmel's present 0.35 µm BiCMOS SiGe Design Kit. The goal was to develop an EDA platform which supports a completely scalable inductor model, including design, layout, and simulation, with seamless integration into the present Cadence® Design Environment, comprising Analog Artist®, Diva®, and Virtuoso® tools.

The HELMET software was incorporated into both the on-chip (SiGe) and in-package inductor design flows, with the later marketed by Atmel as PiiP™ (Passives integrated into Packaging) [1]. The substrate chosen for the PiiP development work was a multi-layer glass ceramic (LTCC) with copper interconnects offered by Kyocera Corporation [2].

HELMET's design environment is depicted in Figure 2. Circular, rectangular, or octagonal spiral inductor geometries are generated using the automated p-cell tools within a layout cellview (Virtuoso). Verification and simulation is accomplished with a two-step process: First, an 'Extracted Cellview' is produced through DIVA Extract which will be used during the LVS verification process. Second, typical, compact, and corner Spectre® and HSpice® models are generated during the 'Extract Full Circuit Model' process. A symbol cellview is also produced that can be used in the schematic view for subsequent analog simulations.

The Diva Extract feature can also be used for the verification of the entire circuit layouts containing HELMET inductive elements. Layout-vs-Schematic (LVS) checks are enabled since inductors are recognized as circuit elements (and not as short-circuits on a metal layer). A quick extract option is available in the 'Layout Cellview' to allow the designers to quickly verify inductor performance over frequency. The results (L and Q values) are automatically displayed in the waveform window, within the Analog Artist environment.

A 2.5 turn rectangular LTCC inductor design example is shown in Figure 3. A pull-down menu within the Virtuoso Layout Environment allows designers quick creation of

either the Atmel on-chip inductor or the in-package LTCC inductor. The physical aspects of the spiral are then entered into the pop-up menu—size, number of turns, width, space, and LTCC metal layer.

A quick performance check of inductance and Q can be enabled from the layout editor (Figure 4). This allows the designer to perform fast design iterations on the physical geometry.

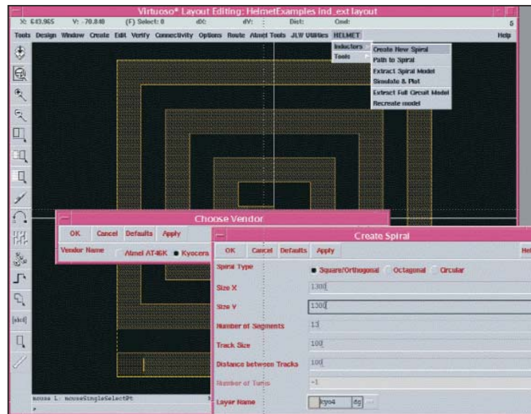

Figure 3 · LTCC spiral creation example.

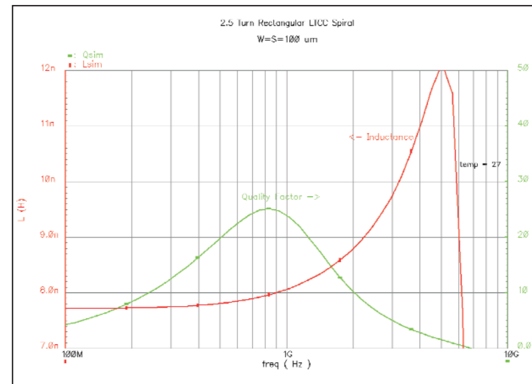

Figure 4 · Plot showing inductance and quality factor (Q) of the spiral.

Advantages for RF IC design

When combined with semiconductor design techniques, advanced passive integration can yield some innovative results. Examples include:

- Orientation of on-chip and in-package inductors can be optimized in every RF design since effects of mutual coupling among many passives can be modeled in near real-time
- Interstage matching circuits with high-Q components can be optimized for in-package solutions
- Circuit Qs of >50 can be achieved with in-package passives thus permitting low phase noise VCOs without external resonators
- Multiple filters and resonators can be configured to permit multi-band operation
- Power amplifier input and output matching circuits can be configured in the semiconductor package and/or the die eliminating the need for external matching.
- Integrated baluns can be built, permitting excellent balanced mixer performance and common-mode rejection.

HELMET enables highly integrated radio products with superior performance, miniaturized size, increased manufacturing yields and dramatically lower costs. Performance is enhanced because much of the complexity is of RF system simulation has been mitigated by HELMET's modeling approach.

Power consumption is reduced because interstage impedance matching can now be accomplished in the package due to the fabrication of high-Q devices. The size is reduced because many of the necessary passive components are now included in the package metal layers and/or on the semiconductor die. Manufacturing yields at the board level are increased because "system yield" begins to correlate to "component yield." The cost drops as passives are eliminated and yield improves.

Design examples

The following designs were realized using HELMET and were fabricated with ATMEL's AT46000 (SiGe BiCMOS) and PiiP-Kyocera process flows.

1) CMOS FET ring mixer with in-package baluns and matching network—Two bandpass baluns were configured to feed the RF and LO ports of a FET-ring passive mixer, which was fabricated using Atmels 0.35 µm SiGe BiCMOS process.

Many previous integrated FET-ring mixers [3, 4] have been limited to broadband operation or expensive discrete baluns, but this test design proves the viability of high-performance, low-cost bandpass devices.

For the RF and LO port baluns, a spiral-type methodology was used (Figure 5). Spiral-type tuned baluns are highly efficient in terms of board area, for frequencies in the few GHz range [5]. The fabricated module and the layout of the LTCC package substrate are shown in Figure 6.

Figure 7 shows the return loss measurements, compared against simulation results obtained with use of the HELMET modeling tool. Even though this was a narrowband design, excellent prediction of resonance frequencies was established, proving the accuracy of the modeling and design approach. The measured responses are slightly "lower-Q" than simulation, mainly due to the losses on the FR4 material used for the evaluation board.

In a FET-ring mixer, the IP3 is mainly a function of the switch transition time. The transition time is mainly a function of the LO voltage,

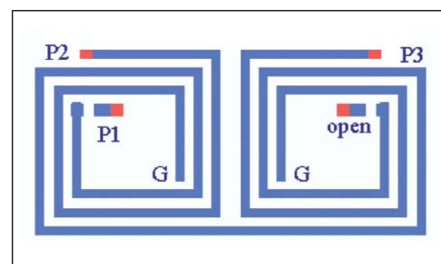

Figure 5 · Spiral-type balun.

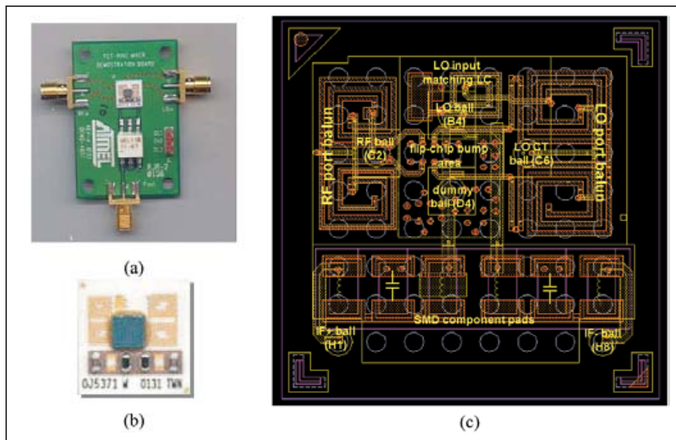

Figure 6 · Ring mixer module: (a) Evaluation board; (b) LTCC module detail; (c) Silicon-LTCC layout view.

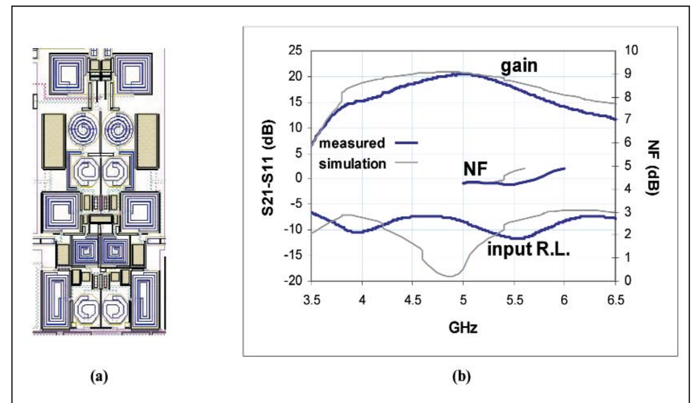

Figure 8 · Fabricated SiGe BiCMOS LNA: (a) layout; (b) comparison of measurements with HELMET-enabled simulation.

and in the case of a resonant drive, the Q of the resonant circuit. For a given LO power, the higher the Q, the higher the IP3. Higher Q, in turn, requires higher tolerance processes and more accurate design and simulation tools. The measured results in Figure 7 were from a first test run, dramatizing the accuracy and applicability of the design tool.

2) 5 GHz SiGe BiCMOS LNA— Another design experiment was the design of a wideband LNA centered near 5 GHz, targeting ISM and WLAN applications. The design relies on the extensive use of integrated spirals on SiGe (Figure 8a), as well as Metal-Insulator-Metal capacitors, for effecting input, output and inter-stage impedance matching and achieving wideband performance.

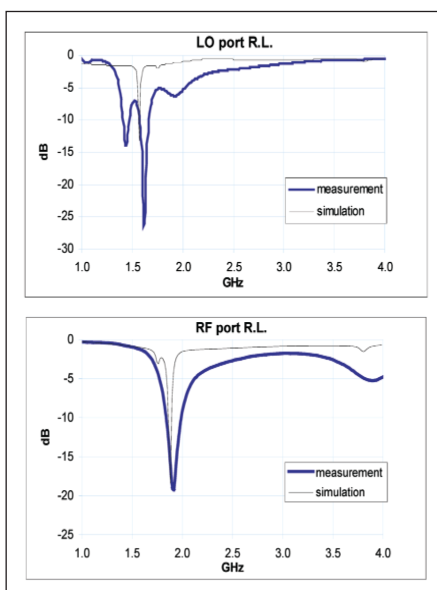

Figure 7 · LO and RF port return loss measurement vs. simulation.

Equipped with HELMET's design environment, Helic's engineers were able to deliver final layout for the LNA in just ten days from project start. Measured results are provided in Figure 8b, compared to simulations using HELMET and Atmel's SiGe BiCMOS Design Kit. A gain of over 20 dB and a noise figure of 4.3 dB were measured at 5 GHz, exactly as predicted by simulation. The discrepancies in input return loss are attributed to wafer probe effects and are not significant, since return loss remains better than 8 dB from 4.9 to 6 GHz. An important first-silicon success was thus established, in record design time.

Conclusion

An integrated-passives-based design methodology was presented, to tackle demanding RFIC design projects. A fast and efficient modeling platform for integrated inductors on-silicon and in-package was presented as a necessary complement to silicon and LTCC process design kits. Using the modeling platform in conjunction with standard RF IC CAD tools, i.e. Cadence, near-optimum results in RFIC and system-in-package designs were demonstrated. Furthermore, these near-optimum designs are often realized on first silicon runs. Standard tools used with HELMET become a complete RF system design and simulation platform, with simulation speeds measured in seconds, not hours or days.

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